In the Claims:

1. (Original) A buffer~~n apparatus for preventing buffers used to reduce delays on relatively long conductive signal lines~~ of an integrated circuit (IC) ~~from being damaged during manufacturing of the IC, the apparatus~~ the buffer comprising:

a first inverter~~buffer~~ having an input connected to one of said conductive signal lines of an IC that comprises the buffer;

a second inverter having an input connected to an output of the first inverter; and

a protection diode ~~comprised by said buffer, the protection diode being coupled~~ connected to the input of the ~~buffer~~first inverter, the protection diode pulling at least some electrical charge off at least one gate of at least one transistor of the first inverter~~of one or more transistor gates of one or more respective transistors of the buffer~~ to prevent the buffer from being damaged by too much electrical charge collecting on ~~one or more~~ the transistor gates ~~of respective transistors of the buffer~~.

2. (Cancelled)

3. (Cancelled)

4. (Currently Amended) The ~~apparatus~~buffer of claim 1, wherein the size of the protection diode in terms of area is at least partially dependent on the ~~gate~~ area of ~~at least one of~~ the transistor gates ~~of the buffer that is available for storing electrical charge~~.

5. (Currently Amended) The ~~apparatus~~buffer of claim 1, wherein ~~each buffer comprises two inverters, each inverter comprising at least one~~ the first and second inverters each comprise a P field effect transistor (PFET) and ~~at least one~~ an N field effect transistors (~~P~~NFETs~~), each PFET and each NFET having a gate a source and a drain, and wherein electrical charge collects on the gates of at least the PFET and NFET of at least one of the inverters~~.

6. (Currently Amended) The ~~apparatus~~buffer of claim 1, wherein each ~~buffer comprises two~~ inverter~~s~~ comprises at least one~~that utilize~~ bipolar junction transistor (BJT)~~ technology~~.

7. (Currently Amended) The buffer~~apparatus~~ of claim 1, wherein the size of the protection diode in terms of area is at least partially dependent on dimensions of the conductive signal line to which the ~~buffer~~ input of the first inverter is connected.

8. (Currently Amended) The ~~apparatus~~buffer of claim 1, wherein the size of the protection diode in terms of area is dependent on dimensions of the conductive signal line to which the ~~buffer~~ input of the first inverter is connected and on the gate area of ~~at least one of the~~said transistor gate~~s~~ of the first inverter~~buffer that is available for storing electrical charge~~.

9. (Currently Amended) The buffer~~apparatus~~ of claim 1, wherein the size of~~for~~ the protection diode in terms of area depends at least partially on the IC process used to design the IC.

10. (Currently Amended) A method for preventing buffers used to reduce delays on relatively long conductive signal lines of an IC from being damaged due to electrical charges that collect on the buffers during manufacturing of the IC, the method comprising the steps of:

buffering at least one ~~of said relatively long~~ conductive signal line~~s~~ of an IC with a buffer to reduce delays in the ~~said one of said relatively long~~ conductive signal line~~s~~, said buffer comprising first and second inverters, the first and second inverters, the buffer including a protection diode connected to an input of the first inverter, ~~the protection diode being coupled to an input of the buffer,~~ the protection diode pulling at least some of the electrical charge off of ~~one or more transistor~~at least one gate of at least one transistor of the first inverter ~~s of one or more respective transistors of the buffer~~ to prevent the buffer from being damaged by too much electrical charge collecting on ~~one or more~~ said transistor gate~~s of respective transistors of the buffer~~.

11. (Currently Amended) The method of claim 10, wherein the buffering step includes buffering multiple conductive signal lines of the IC with buffers, and wherein every buffer of the IC comprises first and second inverters and a protection diode connected to an input of the first inverter.

12. (Currently Amended) The method of claim 10, further comprising the step of determining whether a buffer needs a protection diode prior to buffering one of said conductive signal lines with a buffer that includes a protection diode ~~before including a protection diode in the buffer, wherein only buffers of the IC that have been determined to need protection diodes comprise a protection diode~~.

13. (Currently Amended) The method of claim 10, wherein the size of the protection diode in terms of area is at least partially dependent on the gate area of ~~at least one of the~~said transistor ~~gates of the buffer that is available for storing electrical charge~~.

14. (Original) The method of claim 10, wherein the size of the protection diode in terms of area is preselected.

15. (Original) The method of claim 10, wherein the IC is manufactured using bipolar junction transistor process technology.

16. (Currently Amended) The method of claim 10, wherein the IC is manufactured using field effect transistor process technology.

17. (Currently Amended) The method of claim 10, wherein the size of the protection diode in terms of area is at least partially dependent on dimensions of the conductive signal ~~line to which the buffer input is connected~~.

18. (Currently Amended) The method of claim 10, wherein the size of the protection diode in terms of area is dependent on dimensions of the conductive signal line to which the buffer input is connected and on the gate

area of ~~at least one of the~~said transistor~~ gates of the buffer that is available for storing electrical charge~~.

19. (Original) The method of claim 10, wherein the size for the protection diode in terms of area depends at least partially on the IC process used to design the IC.

20. (Original) The method of claim 11, wherein the size for the protection diode in terms of area is preselected.

21. (New) A method for use in designing an integrated circuit (IC) comprising:

inserting buffer cells into an IC design such that respective inputs of the respective buffer cells are connected to conductive signal lines of the IC design, each buffer cell including:

first and second inverters, the first and second inverters each having at least a non-inverting transistor and an inverting transistor with gates electrically coupled together, an output of the first inverter being connected to an input of the second inverter; and

a protection diode connected to an input of the first inverter.